



Advanced Computer Architecture (New) (1310)

P. Pages : 2

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answer sheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Answer **any two** subquestions from each unit
5. Assume suitable data if necessary.
6. Figures to the right indicate full marks.
7. Non programmable calculator is allowed.

UNIT - I

1. a) What do you mean by program flow mechanism Explain various program flow mechanism. **10**

Define following Network properties and also give their formula for completely connected Network. **10**

- i) Node degree
- ii) Bisection width
- iii) Number of links
- iv) Network diameter

- c) A 40MHZ processor was used to execute of benchmark program with the following instructions mix and clock cycle counts **10**

Instruction type	Instruction count	clock cycle count
instruction arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate and execution time for this process.

UNIT - II

2. a) Explain s - access memory scheme along with neat diagram. **10**
- b) What do you mean by linear pipeline processor ? Also discuss various models of linear pipeline units. **10**

- c) Draw and explain addressing, timing arbitration and interrupts of backplane bus system. **10**

UNIT - III

3. a) Consider the five stage pipelined processor specified by the following reservation table. **10**

	1	2	3	4	5	6
S1	x					x
S2		x				
S3			x		x	
S4				x		
S5	x					x

- What are forbidden latencies ?
 - Draw state transition diagram ?
 - List all the simple cycles & greedy cycles.
 - Determine the optimal constant latency cycle and minimal average latency (MAL)
- b) Explain m(J.K) Sorting algorithm on array processor with an example. **10**
- c) Explain Associative search algorithm. **10**

UNIT - IV

4. a) Explain synchronous and asynchronous parallel algorithm. **10**
- b) Explain various features affecting performance of multiprocessing. **10**
- c) Explain processor characteristics for multiprocessing in detail **10**

UNIT - V

5. a) Explain data flow computer with advantages and potential problems of data flow computer. **10**
- b) Explain various issues in shared variable module. **10**
- c) Explain features of language for parallelism. **10**
