



- c) Draw and explain addressing, timing arbitration and interrupts of backplane bus system. **10**

### UNIT - III

3. a) Consider the five stage pipelined processor specified by the following reservation table. **10**

	1	2	3	4	5	6
S1	x					x
S2		x				
S3			x		x	
S4				x		
S5	x					x

- i) What are forbidden latencies ?
- ii) Draw state transition diagram ?
- iii) List all the simple cycles & greedy cycles.
- iv) Determine the optimal constant latency cycle and minimal average latency (MAL)
- b) Explain m(J.K) Sorting algorithm on array processor with an example. **10**
- c) Explain Associative search algorithm. **10**

### UNIT - IV

4. a) Explain synchronous and asynchronous parallel algorithm. **10**
- b) Explain various features affecting performance of multiprocessing. **10**
- c) Explain processor characteristics for multiprocessing in detail **10**

### UNIT - V

5. a) Explain data flow computer with advantages and potential problems of data flow computer. **10**
- b) Explain various issues in shared variable module. **10**
- c) Explain features of language for parallelism. **10**

\*\*\*\*\*