3735

ELECTIVE - I
VLSI Design
(New) (1254)

P. Pages : 2

Time : Three Hours   Max. Marks :100

Instructions to Candidates :
1. Do not write anything on question paper except Seat No.
2. Answer sheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Figure to right indicates full marks.
5. Assume data wherever necessary.
6. Pls. Mark question number with specific bit to answer.

UNIT - I

1. Solve **any two**.

    a) Write a program for universal gates in VHDL and Verilog, data flow and behavioral style.   **10**

    b) Compair VHDL and Verilog with respect to operators, ease of design, data type structure.   **10**

    c) Write VHDL and Verilog code for half adder using data and behavioral style.   **10**

UNIT - II

2. Solve **any two**.

    a) Explain structure of selective signal assignment with example.   **10**

    b) Compare If statement and case statement with example.   **10**

    c) Design positive edge trigger JK flip - flop using behavioral style.   **10**

UNIT - III

3. Solve **any two.**

    a) Design 4 bit full adder using structural style modelling. **10**

    b) Draw switch level logic diagram for SR Latch and write code. **10**

    c) Explain functions and procedure. Also compare both of
        them with example. **10**

UNIT - IV

4. Solve **any two.**

    a) Explain package in detail using an example. **10**

    b) Write program to read a integer file using file processing format. **10**

    c) Write program for 2:4 decoder using mixed style modelling. **10**

UNIT - V

5. Solve **any two.**

    a) Explain and Draw the Xiliux Spartan 4000 series FPGA. **10**

    b) Write a short on various Debugging tools. Also give
        advantages of logic Analyzer over simulator. **10**

    c) Explain in detail boundary scan for testing logic circuit. **10**

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