Seat No. | | | | | | |

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मध - 019

Digital Circuits and Logic Design
(1030)

P. Pages : 2

Time : Three Hours **Max. Marks : 100**

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Attempt **any two** subquestions from each unit.
5. Figures to the right indicate full marks.
6. Assume suitable data if necessary.
7. Use of non-programmable calculator is allowed.

UNIT - I

1. a) Draw the circuit diagram of a TTL - NAND gate and explain its working. Also mention its advantage and disadvantages. **10**

b) Explain CMOS logic with neat sketch. Explain how it is used as inverter. **10**

c) Explain operation of ECL OR/NOR gate with neat circuit diagram. List features of ECL family. **10**

UNIT - II

2. a) Design 4-bit binary to gray code converter. **10**

b) Minimize the following expressions using k-map and implement it using basic gates. **10**

i) $F(A,B,C,D) = \sum_m(1, 3, 4, 5, 7, 9, 11, 13, 15)$

ii) $F(A,B,C,D) = \sum_m(0, 1, 5, 9, 13, 14, 15) + d\ (3, 4, 7, 10, 11)$

c) Classify the codes. Explain ASCII code and Hamming code in brief. **10**

UNIT - III

3. a) Design BCD adder using IC 7483 with suitable example. **10**

b) Design full adder circuit using NAND gate. **10**

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c) Write short notes on : 10

i) ALU.

ii) 2 - input Mux and De-Mux.

UNIT - IV

4. a) Design decade ripple counter using J-K flip flop. 10

b) Draw and explain S-R flip flop and J-K flip flop with diagram. 10

c) Explain SISO and PIPO for shift register. State the applications of shift register. 10

UNIT - V

5. a) Design MOD - 6 synchronous counter using J-K f/f. 10

b) Design 3-bit up/down synchronous counter with directional mode control. 10

c) Design sequence generator to generate sequence 1101011. 10

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