

Seat
No.

--	--	--	--	--	--



BEI1302

Digital Circuits and Logic Design (New) (1030)

P. Pages : 3

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Attempt **any two** sub-questions from each unit.
5. Figures to the right indicate full marks.
6. Assume Additional suitable data if required.
7. Use of non-programmable calculator is permitted.

UNIT - I

1. Attempt **any two** sub questions :

- a) i) Define noise margin and explain its significance in digital circuit design. Find out noise margin for low and high logic level of standard TTL family. 5
ii) Define "power dissipation" of a logic circuit. A certain logic gate draws 2.0 mA when its output is High and 3.6 mA when its output is low. Calculate its average power dissipation if it is operated on 50% duty cycle and biasing voltage is +5V. Arrange following series of ICs in ascending order of power dissipation
74 XX, 74LS XX, 74AS XX, 74 ALS XX. 5
- b) What are the advantages of schottky TTL circuit over standard TTL circuit ? Draw the circuit diagram of two input schottky TTL NAND gate and explain its operation compare standard TTL and schottky TTL w.r.t. following parameters -
 $V_{OH}(\min)$, $V_{IH}(\min)$, $V_{OL}(\max)$, $V_{IL}(\max)$. 10
- c) i) Explain with neat circuit diagram interfacing of TTL gate driving CMOS gate. 6
ii) What do you understand from the term - 'positive logic and negative logic' ? 4

UNIT - II

2. Solve any two sub-questions.

- a) What is the difference in binary number and BCD number ? Perform the following subtraction of two BCD numbers using 9's and 10's complement method.

$$\begin{array}{r} 1001 \ 1000 \ 0000 \ 0010 \\ - 1000 \ 1001 \ 0011 \ 0100 \\ \hline \end{array}$$

Verify your answer by converting above two numbers in decimal numbers and calculate difference.

10

- b) Implement excess 3 to BCD convertor using universal gates only. For simplification use k-map method.

10

- c) i) What are the popular error detecting and error correcting code ? It is desired to transmit binary word 1011 using even parity Hamming code. At the receiver end 1000101 is received. Find out transmitted information and error if any in the received data.

7

- ii) state and explain Demorgan's theorems.

3

UNIT - III

3. Solve any two sub-questions.

- a) i) Draw the circuit diagram of 4 bit binary adder / subtractor using full adder and explain its operation.

7

- ii) It is desired to implement '8' bit binary adder using two 4 bit binary adders. Draw the circuit using suitable ICs and explain in brief.

3

- b) Write short note on - Look ahead carry generator.

10

- c) i) Implement the following Boolean function using 8:1 Multiplexer.

$$F(A, B, C, D) = \sum m(2, 5, 6, 7, 10, 11, 12, 13, 14).$$

6

- ii) Implement full subtractor using suitable demultiplexer.

4

UNIT - IV

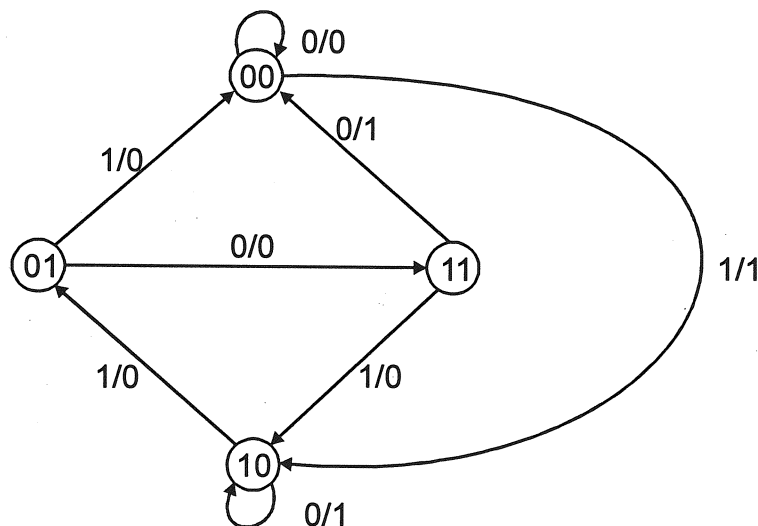
4. Solve any two sub questions.

- a) Explain in brief the basic SR flip-flop. Implement it using 'NOR' gates. Use SR flip flops to design J-K flip flop, D flip flop and T flip flop. 10
- b) Design Mod 8 up-down ripple counter using -ve edge triggered J-K flip flops. Explain its operation with suitable waveforms and truth table. 10
- c) What is universal shift register ? How it differs from bi-directional shift register ? Draw and explain 4 bit universal shift register. 10

UNIT - V

5. Solve any two sub-questions :

- a) A sequential circuit has one input and one output. The state diagram is shown in following figure. Design sequential circuit using 'T' flip flops. 10



- b) Design a Mod-5 synchronus counter using J-K flip flop and implement it. Draw wave form of output of each flip flop, if it driven by 1 KHz, 50% duty cycle clock signal. A series combination of one JK flip flop followed by this counter is constructed. Prepare truth table of resulting circuit. 10
- c) Write short note on sequential generator. 10
