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CEI1330

Electronics Circuit Design (New) (1090)

P. Pages : 4

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. All questions are compulsory & carries equal marks.
5. Assume suitable data if necessary.
6. Unless specified assume used transistor is of silicon.
7. Use of non-programmable calculator is allowed.

UNIT - I

1. Solve any two.

20

- a) Design an unregulated power supply for following requirements.
- i) Bridge Rectifier with capacitor filter.
 - ii) Output D.C. Load voltage of 10V.
 - iii) Output D.C. Load current of 50 mA.
 - iv) Ripple factor of 3%.
 - v) Take $R_s = R_f = 5\Omega$ and also find out the surge current Ratings of the Diodes.
- b) Design Boost Regulator using LM 2577 | 1577 I.C. for $V_o = 20V$, $I_L = 0.6A$, $V_{in} = 8V$, at $60^\circ C$. Design should include external components around I.C. & Heat sink calculations if required.
Take $\Delta I = 25\%$ I_{indavg} for LM 2577 | 157 : \rightarrow

I_{supply}	R_{ON}	θ_{JA}	θ_{CS}	T_j
15 mA	0.25 Ω	65 $^\circ C/W$	2 $^\circ C/W$	150 $^\circ C$

- c) Design a Regulated power supply using Three-terminal Regulator LM 340 for $V_o = 12V$, $I_L = 0.5$ amp at $35^\circ C$.

Design should include, the unregulated power supply section for

$$V_{r(p-p)} = 1.2V.$$

Also find out if heat sink to the I.C. is required or not :

for LM 340

Drop out voltage	T_j	θ_{JA}	θ_{JC}	θ_{CS}
3 V	$150^\circ C$	$35^\circ C/W$	$2.3^\circ C/W$	$2^\circ C/W$

UNIT - II

2. Solve any two.

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- a) Design a single stage common Base amplifier for
 $A_v \geq 50$, $R_i \geq 75\Omega$, $R_{LW} = 50k\Omega$, $R_S = 50\Omega$, $S = 10$, Q points [1mA, 3V]
 Assume used transistor have $h_{fe} = 100$, $h_{ie} = 10k$.
- b) Design single stage common source amplifier with Bypassed source resistance for (i) $A_v \geq 80$ (ii) $R_i \geq 500k\Omega$ (iii) Q points = $I_{DQ} = \frac{1}{2}I_{DSS}$,
 $V_{Dsq} \geq 3V$ (iv) $R_S = 0.5k\Omega$, $R_{LW} = 100k\Omega$, $f_L = 20Hz$
 (v) Take $V_{RD} = V_{R3}$ R_3 is the source resistance of device. FET used have $I_{DSS} = 2mA$, $V_P = -5V$, $g_{mo} = 12mS$ $r_d = 80k\Omega$.
 Use potential Divider Bias Network.
- c) Design a single stage C.E. amplifier with [partially bypassed and partially unbypassed Emitter Resistance] for
 $A_{VS} \geq 50$, [Q points : $I_{CQ} = 1mA$, $V_{CEQ} \geq 5V$]
 $R_i = 10k\Omega$, $S = 10$, $R_{LW} = 100k\Omega$, $R_S = 0.6k\Omega$
 BJT have $h_{fe} = 200$, $h_{ie} = 10K$.

UNIT - III

3. Solve any two.

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- a) Design of class-A transformer coupled amplifier to deliver 45 mw of a.c. power to the load resistance of 4Ω , Take $V_{CC} = 9V$ and efficiency of X'mer as 70%.
- b) Design a class-B transformer coupled power amplifier for $P_{ac} = 10W$, $R_L = 5\Omega$, $n_{transformer} = 80\%$, $S = 8$, $V_{CC} = 20V$.
- c) Design a complementary symmetry power amplifier for $P_{ac} = 0.5W$, $R_L = 8\Omega$, frequency response 30 Hz to 10 kHz. Used transistors have $h_{fe} = 120$.

UNIT - IV

4. Solve any two.

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- a) Design a monostable multivibrator to provide a pulse of $300\mu\text{sec}$, with amplitude of output is 9V, used BJT have $h_{fe} = 100$, $I_{cq} = 1\text{mA}$.
- b) Design a Colpitt oscillator using FET (n-channel) (with potential Bias N/W) for
 - i) freq. of oscillation $f_o = 5\text{MHz}$
 - ii) Voltage gain $A_v = 25$, $R_i = 200K\Omega$
 - iii) Q points : $I_{Dq} = 1\text{mA}$, $V_{Dsq} = 5V$.
 - iv) Voltage across source resistance R_3 of Device $V_{R_3} = 3V$
 - v) Take inductor in feedback Network equals to $1\mu\text{H}$.
 FET used have $I_{DSS} = 2\text{mA}$, $V_p = -6V$, $r_d = 50K\Omega$, $g_{mo} = 3\text{m}\Omega$.
- c) Design a Tuned Amplifier using FET for
 - i) Resonance frequency $f_o = 5\text{MHz}$
 - ii) Bandwidth = 125 KHz
 - iii) Overall voltage gain = 116
 - iv) I/P Resistance = $500K\Omega$

- v) Q points : $I_{DQ} = \frac{1}{6} I_{DSS}$, $V_{DSQ} \geq 5V$.
- vi) Take $V_{DS} = V_{R_3}$ (R_3 is the source Resistance of Device)
- vii) $R_{LW} = 100K\Omega$, $R_S = 50K\Omega$.
- Use potential Divider Network FET used have
- $I_{DSS} = 20mA$, $V_P = -2V$, $r_d = 50K\Omega$, $C_o = 2.5pf$.

UNIT - V

5. Solve any two.

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- a) Design a Band pass filter for $f_L = 600Hz$, $f_H = 6KHz$ with attenuation Rate of 40 dB/decade in stop-band. Also take pass-band as flatt as possible. Use salen-key equal component approach. [Take value of capacitor as 0.01 μf]
- b) Design AC amplifier using 741-C with single ended power supply for
- Inverting mode
 - $A_f = 10.5$
 - $R_{if} \geq 20K$ $R_S = 75\Omega$
 - $V_{CC} = +24V$, $I_L \leq 2mA$ $f_L = 20Hz$
- 741-C have following specifications -
- $A_o = 2 \times 10^5$, $f_o = 5Hz$, $R_i = 2M\Omega$, $R_o = 75\Omega$, S.R. = 0.5V/ μ sec.
- c) Design H.P.F. using 741-C
- Order of filter \rightarrow 4th
 - Overall gain \rightarrow 10
 - Bessel Response (Assume C \rightarrow 0.01 μf)
 - $f_o = 9KHz$.
- For Bessel filter use data

Filter order	Sections	Parameters
4 th order	I st (2 nd order)	$\alpha = 1.916$ $K_{LP} = 0.696$
	II nd (2 nd order)	$\alpha = 1.241$ $K_{LP} = 0.621$
