



Electronics Circuit Design (1090)

P. Pages : 4

Time : Three Hours

Max. Marks : 100

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answer sheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. All questions carry equal marks.
5. Assume suitable data, if required.
6. Unless specified assume material of device of silicon (si)
7. Use of non programmable calculator is allowed.

UNIT - I

1. Solve **any two**.

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- a) Design a boost type switching Regulator using IC 1577/2577 to meet $E_{in} = 5$ volt, $E_{load} = 12$ Volt
 $I_{load} = 800$ mA $\Delta V_{load}(p-p) = 0.05V$
 $\Delta I = 25\%$ of $I_{L\max}$ $\theta_{JA} = 65^\circ C/w$
Draw designed circuit diagram. Design should include calculation of component value and heat sink for IC if required (No need to design unregulated power supply).
- b) Design fold - back protection circuit required to be use with a series regulator for the following requirement.
- i) output voltage $V_O = 10$ V
 - ii) load current $I_L = 500$ milliamp
 - iii) Short circuit current $I_{SC} = 100$ milliamp
 - iv) $V_{in} = 15$ V
 - v) $h_{fe1} = 50$ (series pass transistor)
 $h_{fe2} = 200$ (comparator transistor)
 $h_{fe3} = 50$ (foldback transistor)
- c) Design a regulator using LM 340 - 6T which will provide 6 volt and current upto 500 milliamp at $30^\circ C$. Draw the designed circuit diagram. Draw the designed include selection of transformer calculation of rating of filter capacitor & rectifier diode and heat sink to IC if required.

LM 340 - 6T

i) Dropout voltage = 2V

ii) $\theta_{JA} = 50^\circ\text{C}/\text{w}$ iii) $\theta_{SA} = 7.9^\circ\text{C}/\text{w}$ **UNIT - II****2. Solve any two.****20**

a) Design a single stage JFET amplifier for the following requirement.

i) Voltage gain $A_V = 25$, $R_i = M\Omega$ ii) Q point ($I_{DSS}/2$, 12 V) using self biasiii) $f_L = 20\text{ Hz}$ iv) Phase shift $\phi = 180^\circ$

draw the designed circuit diagram. Design should include bias component and external coupling capacitor use n channel JFET with $I_{DSS} = 2\text{ mA}$, $V_P = -6\text{ V}$, $g_{mo} = 0.3\text{ S}$, $r_d = 50\text{ k}\Omega$

b) Design a single stage amplifier in C. E. configuration with emitter by passed for the following requirements.

i) Voltage gain $A_V \geq 100$ ii) Stability factor $s = 6$

iii) Q point (1 mA, 3V)

iv) $R_i = 5\text{ K}\Omega$ v) $f_L = 20\text{ Hz}$ $f_H = 20\text{ KHz}$ vi) $R_{LW} = 100\text{ K}\Omega$, $R_S = 600\Omega$ (source resistance)

use transistor (BJT) having

 $h_{fe\text{ min}} = 200$, $h_{ie} = 10\text{ K}\Omega$, $f_T = 10\text{ MHz}$

Draw the designed circuit diagram? Design bias component and external capacitor.

c) Design voltage series feedback amplifier (Two Stage) for following specification.

i) $A_V f \geq 120$, $R_{LW} = 5\text{ K}\Omega$, $V_{CC} = 12\text{ V}$ ii) $V_O = 6\text{ volt}$ (P - P)

iii) Q point for both stage (2mA, 5V)

iv) Stability factor $S = 10$

Design must include bias component (no need to design external capacitor). Draw designed circuit diagram.

Use BC 109 transistor with $h_{fe\text{ min}} = 200$, $h_{ie} = 2.6\text{ K}\Omega$ **UNIT - III****3. Solve any two.****20**

a) Design a transformer coupled class A power amplifier for

i) $V_o = 4\text{ V Crms}$ ii) Stability factor $S = 8$

- iii) $V_{cc} = 15 \text{ V}$
 - iv) $R_L = 4 \Omega$
 - v) $\eta = 0.9$
use BJT with $h_{fe} = 100$
- b) Design class B transformer coupled audio power amplifier to give output power of 10 W to a resistive load of 4Ω . Efficiency of output transformer is 80%, $S = 8$, $V_{cc} = 18\text{V}$. Design must include calculation of transistor rating, bias component and transformer selection use $h_{fe} = 25$.
- c) Design complementary symmetry power amplifier for $P_{ac} = 0.5 \text{ W}$, $R_L = 8 \Omega$, frequency Response 30 Hz to 10 KHz. Design must include driver circuit transistor used in complementary stage use $h_{fe} = 120$

UNIT - IV

4. Solve any two.

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- a) Design a colpitts oscillator using JFET for the following requirements.
- i) Frequency of oscillation $f_o = 1\text{MHz}$
 - ii) Voltage gain $A_V = 50$
 - iii) A point $[I_{DSS} / 2, 12 \text{ V}]$
 - iv) $R_i = 1 \text{ M}\Omega$
 - v) $L = 1 \mu\text{H}$
- Draw the designed circuit diagram.
Design must include bias component and coupling capacitor values.
use FET 2 N 3822 with $I_{DSS} = 2\text{mA}$, $V_P = -6\text{V}$
 $g_{mo} = 3 \text{ m}\Omega$, $r_d = 50 \text{ K}\Omega$.
- b) Design a transistorised collector coupled monostable
- i) Pulse width of $250 \mu \text{ sec}$, $V_o = 10 \text{ V}$
- Draw the designed circuit diagram.
design must included calculation of external components required for the circuit
use $I_C = 2 \text{ mA}$, $h_{fe} \text{ min} = 50$
- c) Design a single tuned amplifier using FET (Nchannel) for following requirement.
- i) Voltage gain at resonance $A_V = 100$
 - ii) Resonant frequency $f_o = \text{MHz}$
 - iii) Q Effective = 15
 - iv) $R_i = 1 \text{ M}\Omega$
 - v) Bias requirement is set at $I_{Dq} = I_{DSS}/2$, $V_{DSq} = 8\text{V}$ with $V_{DD} = 20\text{V}$,
 $v_p = -6\text{V}$, $g_{mo} = 5 \text{ m}\Omega$, $r_d = 50\text{K}$, $I_{DSS} = 7 \text{ mA}$.

UNIT - V

5. Solve **any two**.

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a) Design a band pass filter circuit for the following requirement.

i) $AV = -9$ ii) $FC = 60 \text{ Hz}$ iii) $Q = 20$ iv) Roll of rate $60 \text{ dB} / \text{decade}$.b) Design non inverting amplifier with single supply of $+15 \text{ V}$ using OPAMP for the following requirementi) voltage gain $AV = 50$ ii) $FL = 20 \text{ Hz}$ iii) $IL = 5 \text{ mA}$

use the specification of IC 741 C

Draw the designed circuit diagram.

c) Design an Active filter using sallen - key. Unity gain low pass filter satisfy the following requirement.

i) Roll of rate $= 40 \text{ dB} / \text{decade}$

ii) Pass bond flat as possible

iii) Critical frequency 3 KHz

iv) Gain of 6
