Seat No. | | | | | | |

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BEI1305

# Semiconductor Devices and Circuits (New)
## (1050)

**P. Pages : 4**

**Time : Three Hours** **Max. Marks : 100**

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answersheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Attempt **any two** sub questions from each unit.
5. Assume suitable data wherever necessary and state the assumptions made.
6. Diagrams / sketches should be given wherever necessary.
7. Use of logarithmic table, drawing instruments and non programmable calculator is permitted.
8. Figures to the right indicate full marks.

### UNIT - I

**1.** a) What is the meaning of diffusion of charge carrier ? Derive expression for diffusion of 'n' type semiconductor material. Write and explain the expression of total current density in 'n' type semiconductor material. **10**

b) A bridge rectifier circuit operated on 230V, 50Hz mains supply has following specification -
transformer turns ratio $N_p : N_s = 10 : 1$
secondary transformer resistance $R_s = 5\Omega$.
forward resistance of p-n junction diode $R_f = 10\Omega$.
load current variation from 0mA to 100mA.
Calculate :
i) Ripple factor at full load condition.
ii) Rectifier efficiency at no load and full load condition.
iii) Load regulation. **10**

c) i) Find the resistivity of intrinsic silicon. If it is doped with pentavalent impurity to the extent of 1ppm, what will be its resistivity. Following data may be used. No. of $S_i$ atoms = $4.96 \times 10^{22}/cm^3$, Ni = $1.52 \times 10^{10}/cm^3$
$q = 1.6 \times 10^{-19}$ Coulomb, $\mu_n = 0.135 m^2$/volt - sec
$\mu_p = 0.048 m^2$ / volt - sec. **5**

ii) Explain in brief "Junction Capacitances" **5**

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## UNIT - II

2. a) i) Justify the necessity of biasing for transistor circuit. **5**

ii) Discuss the methods or techniques used to increase input impedances in transistor circuits, typically $Z_i > 1\ M\Omega$ **5**

b) Transistor used in the C. E. amplifier circuit of fig. 1, has output characteristics as shown in fig. 2. If transistor of fig. 1 is a Si transistor having $\beta = 55$; determine

i) Operating point using graphical method.

ii) Operating point by knowing $\beta = 55$. **10**

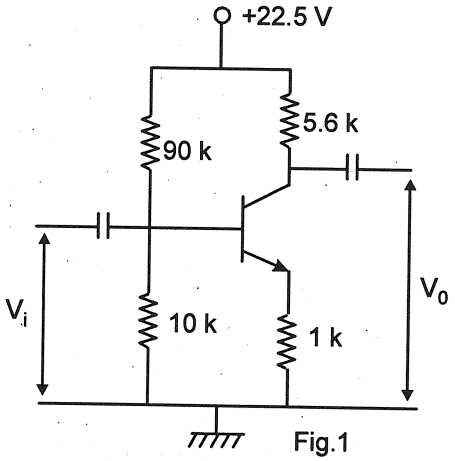


Fig.1

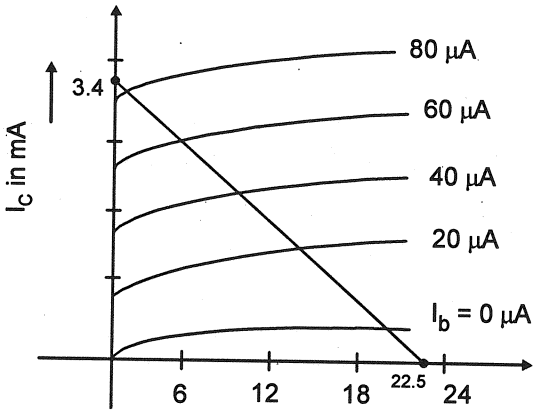


Fig.2

c) For the amplifier shown in fig. 3, calculate Ri, Ri', Av, Avs and $A_I = -I_2 / I_1$. Use the following data. hie = 1.1K, hfe = 50, hre = $2.5 \times 10^{-4}$, hoe = 24 μA / V Explain in brief the theorem or concept used by you for the analysis of the circuit. **10**

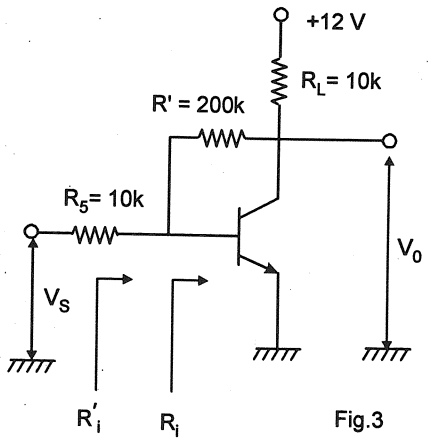


Fig.3

## UNIT - III

3. a) Explain 'Pinch OFF Voltage' and 'Pinch OFF Region' w.r.t. JFET. For a n channel silicon JFET with 2a = channel width = $6 \times 10^{-4}$ cm and ND = $10^{15}$ electrons /$cm^3$, find pinch OFF voltage and the channel half width 'b' for $V_{GS}$ = ½ VP and $I_D$ = 0. (Assume $\epsilon_0 = \left(36\pi \times 10^9\right)^{-1}$. **10**

b) Define 'transconductance' of JFET. How it can be obtained from transfer characteristic ? Derive mathematical expression for transconductance. Determine the value of transconductance and drain current at $V_{GS}$ = - 4V, if JFET data sheet includes. $I_{DSS}$ = 20mA, $V_p$ = - 8V, $g_{mo}$ = 5000 μA / V . **10**

c) The amplifier circuit of fig.4 uses an n channel JFET for which $V_p$ = -2.0V, $I_{DSS}$ = 1.65mA. It is desired to bias the circuit at $I_D$ = 0.8mA. Assume $r_d >> R_d$ and find (i) $V_{GS}$ , (ii) $g_m$ , (iii) $R_S$ (iv) $R_d$

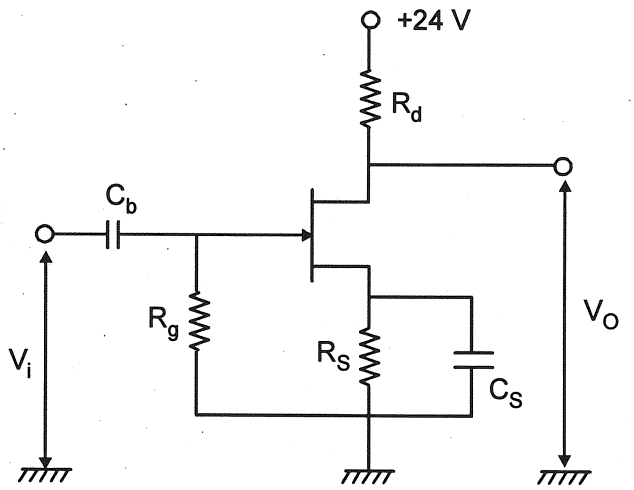


Fig.4

Suggest suitable modification in above circuit so that its operating point remain stable against device variations. **10**

## UNIT - IV

4. a) What is depletion type MOSFET ? Explain its performance with the help of drain and transfer characteristics. **10**

b) i) Write short note on - "Handling precautions of CMOS devices". **5**

ii) The data sheet for certain enhancement type MOSFET reveals that $I_{D(ON)}$ = 12mA at $V_{GS}$ = -12V and $V_{GS(th)}$ = - 3.5 V. State whether device is an 'n' channel or a p channel. Find the value of $I_D$ when $V_{GS}$ = -7V. Also determine the required value of $V_{GS}$ so that drain current can be 6 mA. **5**

c) The 'e' MOSFET shown in fig '5' has $V_T$ = 2V, $\gamma_d = 75\,K\Omega$, $g_m$ = 1.4mA/V. It is biased at 1.9mA. Verify the biasing of MOSFET and calculate its voltage gain $\left(A_{VS} = {}^{V_O}/_{V_S}\right)$ and input resistance ($R_i$) **10**

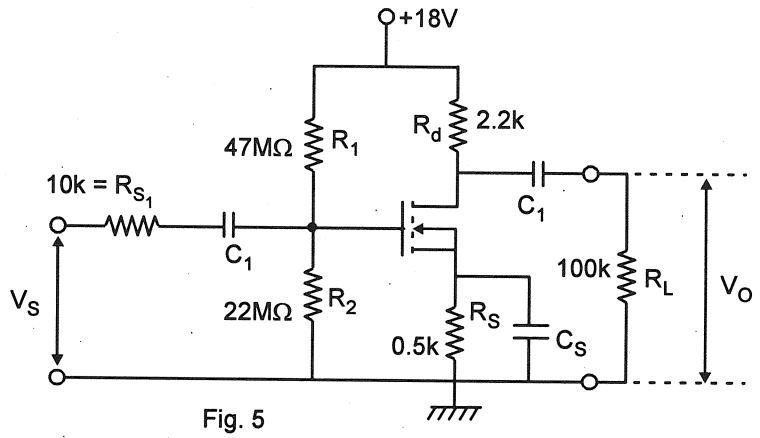


Fig. 5

## UNIT - V

**5.** a) Draw the circuit diagram of CMOS invertor and explain its operation. What is noise margin and threshold voltage ? **10**

b) i) It is desired to have a lower 3 dB frequency of not more than 10Hz for an R - C coupled amplifier for which output resistance of earlier stage (Ry) is 1 KΩ. What minimum value of coupling capacitor is required if (x) FET of $R_g$ = 1M; (y) transistor with $R_i$ = 1 KΩ and $1/h_{oe}$ = 40 KΩ are used. **5**

ii) If number of amplifier stages are cascaded then explain the effect on overall frequency response of cascaded amplifier. **5**

c) Explain step response of an amplifier circuit and define rise time and sag. What is co-relation between rise time and higher cut off frequency of an amplifier circuit. It is desired to pass 50Hz square wave signal with less than 10% sag, what should be the maximum allowed lower cut off frequency. **10**

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