* 4 0 4 5 *

Solid State Devices Circuits - I
(143101 / 183101 / 233101)

P. Pages : 4

Time : Three Hours **Max. Marks : 80**

Instructions to Candidates :
1. Do not write anything on question paper except Seat No.
2. Answer sheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Answer **any two** sub questions from each question.
5. Assume suitable data if necessary.
6. Use of non-programmable calculator is allowed.

UNIT – I

1. a) Define drift and diffusion current. A bar of n type silicon has length of 4 cm and circular cross section of 10 mm^2 when it is subjected to a voltage of 1 volt applied across its length, the current flowing thro' it is 5 mA. **8**

Calculate : i) Concentration of free $\overline{e}$

ii) Drift velocity of $\overline{e}$

Assume charge of electron = $1.6\times10^{-19}C$

mobility μ = $1300cm^2/V-S$

b) State mass – action law. Find out the conducting of Si for **8**

i) Intrinsic condition at room temp.

ii) With donor impurity of 1 in 10^8

iii) With acceptor impurity of 1 in 5×10^7

Given : $n_i = 1.5\times10^{10}/cm^3$, $\mu_n = 1300cm^2/V-S$, $\mu_p = 500cm^2/V-S$,

no. of 'Si' atoms = $5\times10^{22}/cm^3$

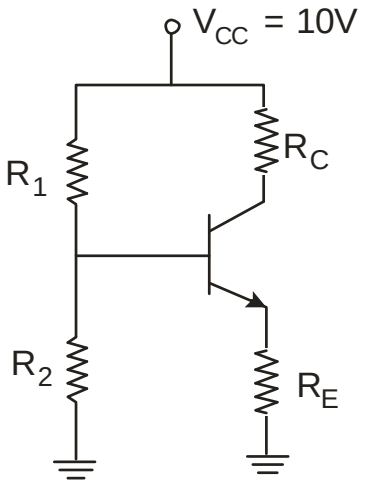
c) Derive expression for ripple factor and efficiency of a full wave Rectifier. **8**

UNIT – II

2. a) Draw h – parameter equivalent circuit for a single stage CE amplifier and derive expressions for Ri, Ai and Av. **8**

b) Explain different bias compensation techniques in detail. **8**

c) Determine the value of IC, V_{CE} and stability factor for the voltage divider bias circuit as shown in fig. **8**



V_{BE} = 0.7V
β = 100

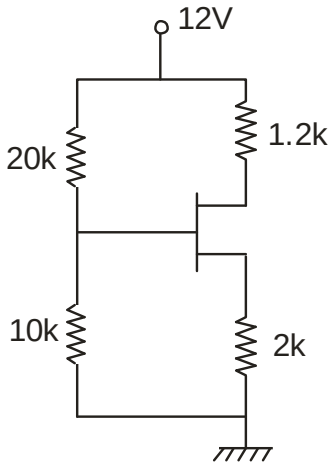
Given :
R_1 = 10 k
R_2 = 5 k
R_C = 1 k
R_E = 500 Ω

UNIT – III

3. a) Explain operation of n-channel JFET with neat diagram. Also draw the drain characteristics curves. **8**

b) Write short notes on FET parameters. **8**

c) For the ckt shown in fig. calculate I_D, V_{GS}, V_G, V_{DS} and V_S. **8**

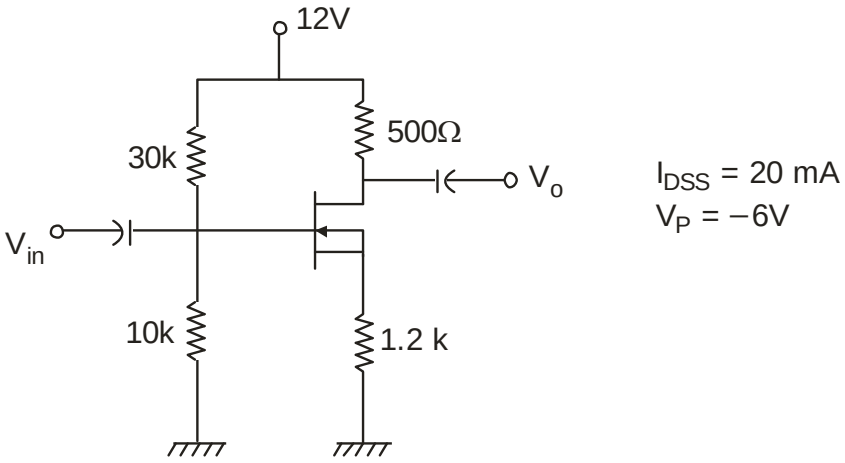


I_{DSS} = 12 mA
V_P = −4V

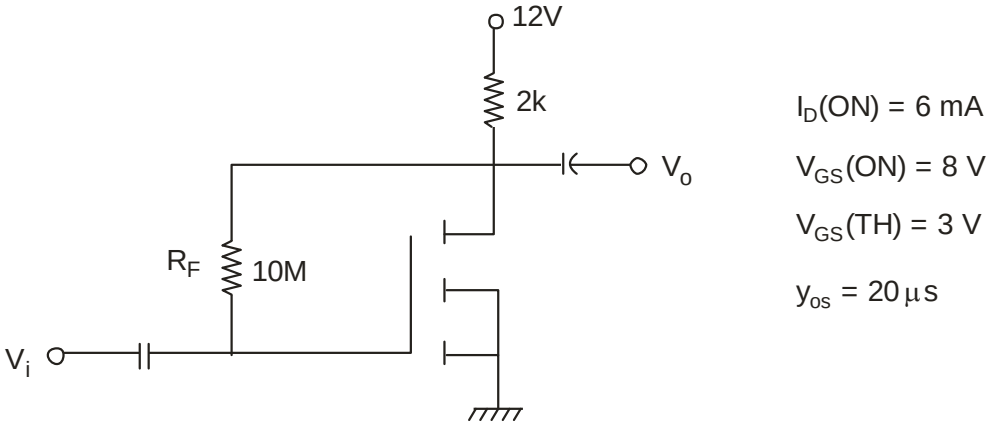
UNIT – IV

4. a) Explain the construction and operation of n – channel enhancement type MOSFET. **8**

b) For the circuit shown in fig. calculate I_D, V_{DS}, V_{GS}, V_S **8**



c) For the fig. shown below calculate gm, rd, Zi, Zo, Av without rd $(R_F \geq rd/R_D, rd \geq 10R_D)$ **8**

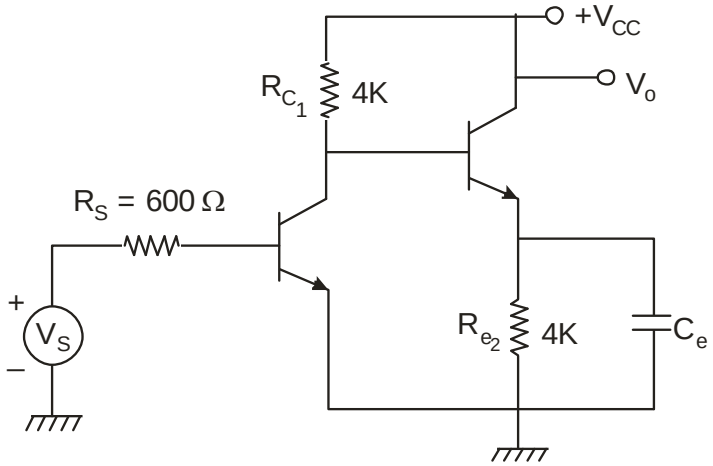


UNIT – V

5. a) Explain square wave testing. Derive equation for f_L and f_H. **8**

b) Explain effect of coupling, bypass and junction capacitor on frequency response of BJT. **8**

c) For the two stage CE – CE amplifier ckt shown in fig. find the overall current gain Ai. The h – parameters of transistor are **8**



h_{ie}= 1600 Ω, h_{fe} = 60

h_{re} = 5 x 10^{-4}, h_{oe} = 25 μ A/v

h_{ic} = 1600 Ω, h_{fc} = – 61

h_{rc} = 1 , h_{bc} = 25μ A/v

****