



**Digital Techniques and Applications**  
**(143103 / 183103 / 233103)**

**P. Pages : 2**

**Time : Three Hours**

**Max. Marks : 80**

Instructions to Candidates :

1. Do not write anything on question paper except Seat No.
2. Answer sheet should be written with blue ink only. Graph or diagram should be drawn with the same pen being used for writing paper or black HB pencil.
3. Students should note, no supplement will be provided.
4. Solve **any two** sub-questions from each unit.
5. Draw neat diagram whenever necessary.
6. Assume suitable data if necessary.
7. Use of non-programmable calculator is allowed.
8. Figures to right indicate full marks.

**UNIT – I**

1. a) i) Convert  $(105)_{10}$  to binary & BCD equivalent. 8  
ii) Explain minterm & maxterm with suitable example.
- b) What do you mean by signed binary numbers ? What are the different methods of representing signed numbers in binary form ? 8
- c) Minimize the following expressions using k-map & implement it using gates. 8  
i)  $F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5,8,14)$   
ii)  $F(A,B,C,D) = \sum m(0,1,5,9,13,14,15) + d(3,4,7,10,11)$

**UNIT – II**

2. a) i) Design & implement full adder using two half adders. 8  
ii) Design & implement 1-bit comparator.
- b) Construct 16:1 mux using 4:1 mux. 8
- c) Design binary to gray code converter. 8

**UNIT – III**

3. a) Differentiate between combinational & sequential circuits. Explain J-K flip-flop using NAND gates. **8**
- b) Convert : **8**
- i) S-R flip-flop to J-K flip-flop.
- ii) J-K flip-flop to T-flip-flop.
- c) Draw & explain 4-bit ring counter. **8**

**UNIT – IV**

4. a) Differentiate between synchronous & asynchronous counter. Draw & explain 4-bit asynchronous counter. **8**
- b) Design & implement decade ripple counter. **8**
- c) Differentiate between moore & mealy machines. Draw & explain moore machine. **8**

**UNIT – V**

5. a) List and explain characteristics of digital ICs. **8**
- b) Draw & explain CMOS NAND gate & CMOS NOR gate. Also write their truth tables. **8**
- c) Explain the operation of 2-input TTL NAND gate. **8**

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